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FPGA Vernier Digital-to-Time Converter With 1.58 ps Resolution and 59.3 Minutes Operation Range

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ABSTRACT

The first FPGA multiple channel digital-to-time converter, or digital pulse generator, is proposed to further extend FPGA applications into analog domain. Based on vernier principle, the effective resolution is made equivalent to the period difference of two phase-locked loop (PLL) outputs. The finer than ever DTC resolution of 1.58 ps is achieved with an Altera Stratix III FPGA chip. The DNL and INL are verified to be -0.086 ~ +0.12 LSB and -0.93 ~ +0.75 LSB respectively for input value varied from 1 to 1026. The widest operation range of 59.3 minutes is accomplished with 51 functioning input bits. Except for 2 shared PLLs, there are only 422 combinational ALUTs and 84 dedicated logic registers utilized per channel for 224-channel circuit implementation. The power consumption per channel is simulated to be 3.04 mW only. With a simple but powerful structure, the design cost is substantially reduced from those of its predecessors.

INDEX TERMS

- **INSPEC**
  - **Controlled Indexing**
    convertors , field programmable gate arrays , phase locked loops , pulse generators
  - **Non Controlled Indexing**
    FPGA Vernier digital-to-time converter , FPGA multiple channel digital-to-time converter , digital pulse generator , logic registers , phase-locked loop , time 59.3 min
- **Author Keywords**
  ATE , BIST , FPGA and vernier principle , digital pulse generator , digital-to-time converter

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