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Field of study: Low Power System/VLSI Design, Embedded system hardware/software analysis and optimization

Key words: VLSI, Embedded system

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1. The Subject and Aims of Research

Low Power SoC Design and Synthesis

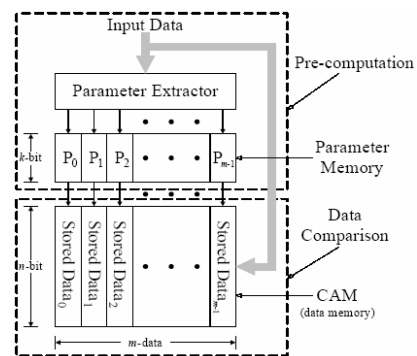
Low Power Image Processing

Low Power Computer Organization and Architecture

2. Related Recent Research Topics

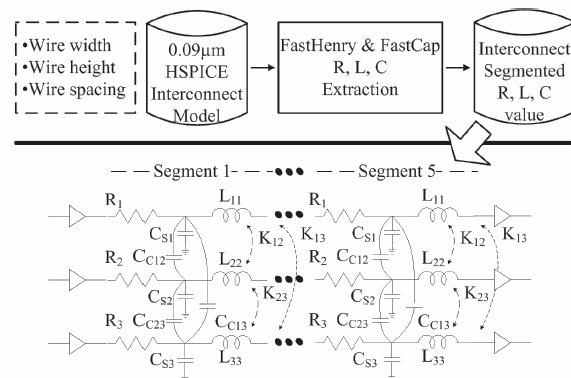
- **Low Power Precomputation- CAM Design**

In this research, we propose an algorithm to synthesize a proper pre-computation circuit based on the Block-XOR architecture for specific data types. Because the Block-XOR architecture is only suitable for random input patterns, we propose a Gate-Block Selection algorithm which can synthesize a proper pre-computation circuit by using different logic gates to reduce the number of comparison operations and further save power consumption. The experimental results showed that our proposed approach effectively reduces 3% to 13% of comparison operations and saves 2% to 10% of power reduction compared with the Block-XOR architecture.



- **Low power Dynamic Bus Design**

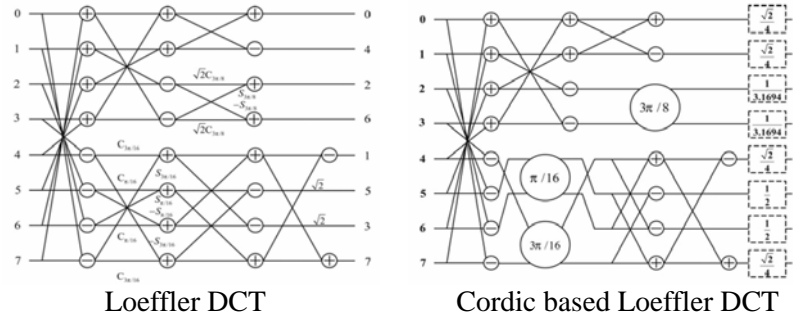
As technology scales down to nanometer technology, coupling effects between neighboring wires become very important. In this research, we propose a low power dynamic bus encoding scheme which simultaneously reduces the capacitive and inductive effects by the measurement of real RLC model. It should be noted that our method does not need a sufficient knowledge of the patterns on the bus. Our experimental results show that the proposed approach can save power consumption of the bus up to 12% compared to the non-encoded case. We also propose an area-aware scheme to optimize our circuits in terms of power consumption and area. The scheme can reduce the circuit area up to 29% while keeping almost the same power reduction.



- **Low Power Cordic Based Loeffler DCT for Signal Processing**

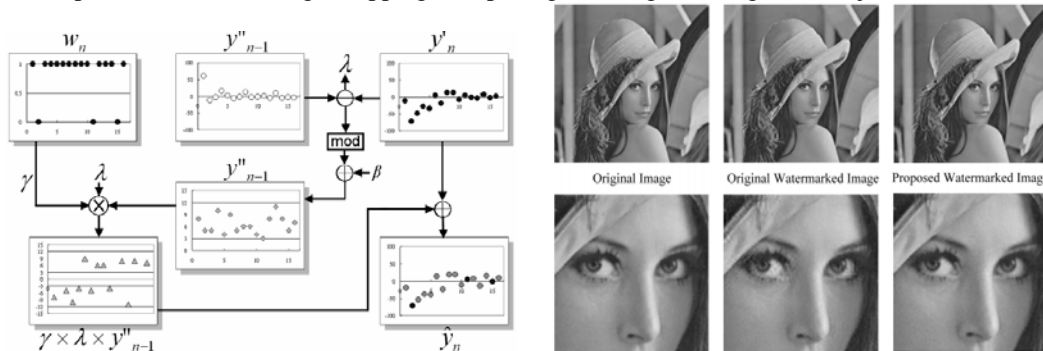
A computationally efficient and high-quality preserving discrete cosine transform (DCT) architecture is presented. It is obtained by optimising the Loeffler DCT based on the coordinate rotation digital computer (Cordic) algorithm. The computational complexity is reduced significantly from 11 multiply and 29 add operations (Loeffler DCT) to 38 add and 16 shift operations without losing quality. After synthesising with TSMC 0.13-µm technology library, Synopsys PrimePower was used to estimate the power consumption at gate-level. The experimental results show that the proposed 8-point one-dimensional DCT architecture only consumes 19% of the area and about 16% of the power of the original Loeffler DCT. Moreover,

it also retains the good transformation quality of the original Loeffler DCT.



- **High Quality Robust Digital Watermarking**

According to Low Power Watermarking Algorithm, we develop a high quality and robust watermarking algorithm that combines the advantages of block-based permutation with that of neighboring coefficients embedding. The proposed approach uses the relationship between the coefficients of neighboring blocks to hide more information into high frequency blocks without causing serious distortion to the watermarked image. In addition, an extraction method for improving robustness to mid-frequency filter attacks is proposed. Our experimental results show that the proposed approach is very effective in achieving perceptual imperceptibility. Moreover, the proposed approach is robust to a variety of signal processing operations, such as compression (JPEG), image cropping, sharpening, blurring, and brightness adjustments.



3. Selected Publications and Projects

Publications:

- (1). Shanq-Jang Ruan, Chi-Yu Wu, and Jui-Yuan Hsieh, "Low Power Design of Precomputation-based Content Addressable Memory," IEEE Trans. on Very Large Scale Integration (VLSI) Systems, Vol. 16, No. 3, pp. 331-335, Mar. 2008. (SCI/EI)
- (2). Shanq-Jang Ruan and Shang-Fang Tsai, "DS2IS: Dictionary-based Segmented Signal Inversion Scheme for Low Power Dynamic Bus Design," Journal of Systems Architecture. (accepted) (SCI)
- (3). C.-C. Sun, Sanq-Jang Ruan, B. Heyne and J. Goetze, "Low-power and high-quality Cordic-based Loeffler DCT for signal processing," IET (IEE)Circuit Devices & System, (6), pp. 453-461, Jan. 2008. (SCI/EI)
- (4). Yu-Ting Pai and Shanq-Jang Ruan, "A High Quality Robust Digital Watermarking by Smart Distribution Technique and effective embedded scheme," IEICE Trans. on Fundamentals, Vol. E90-A, No.3, pp. 597-605, March, 2007. (SCI/EI)
- (5). Shanq-Jang Ruan, Kun-Lin Tsai, Edwin Naroska and Feipei Lai, "Bipartitioning and Encoding in Low Power Pipelined Circuits," ACM Trans. on Design Automation of Electronic Systems, Vol. 10, No.1, Jan. 2005, pp 24-32. (SCI/EI) (NSC 92-2218-E-011-006)

Projects:

- (1). Design and Evaluation of Low Power Image Watermarking Algorithms. (NSC PPP Germany-Taiwan, Jan. 2007- Dec. 2008)
- (2). Low Power and Real Time Design of Precomputation-Based Content Addressable Memory (NSC 96-2221-E-011-171 -)
- (3). Design and Analysis of Low Power Dynamic Bus Based on RLC simulation. (NSC 95-2221-E-011-188 -)