
Introduction

- **Principal Investigator:** Chung-An Shen (沈中安), Assistant Professor
 - **Highest Degree:** PhD in Electrical and Computer Engineering, University of California, Irvine
 - **Affiliation:** Electronic and Computer Engineering (Computer Engineering), National Taiwan University of Science and Technology
 - **Contact:** Office T2 504-3 ; email cashen@mail.ntust.edu.tw
 - **Research Interests:**
 - Algorithms and VLSI architectures for signal processing, with focus on communication and video/image systems
 - Low power architectures and circuits design
 - FPGA designs and applications
 - Embedded system designs and applications
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Signal Processing Systems and Design Challenges

- Applications: communication, video, image, audio, voice, bioelectronics...etc.
- Trends in contemporary and future systems:
 - Increased processing **throughput**
 - Reduced **size** and **power** consumption
- The major challenge for designing efficient signal processing systems:

***The joint development of low-complexity algorithms
and efficient VLSI system architectures:***

Algorithm-Architecture Co-Design

Current Project I^α: Algorithms and VLSI Architectures for Efficient Wireless Systems

➤ Trends in Wireless Systems (LTE, WiMAX, 802.11ac):



- Multi antenna techniques ([MIMO](#))
- Multi carrier Modulation ([OFDM](#))

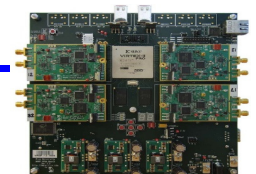


➤ Low power architectures are the key to enable efficient wireless systems:

- Joint [MIMO detection](#) and [Turbo decoding](#): Efficient algorithms and low-power VLSI architectures
- Low complexity designs for [OFDM](#) systems



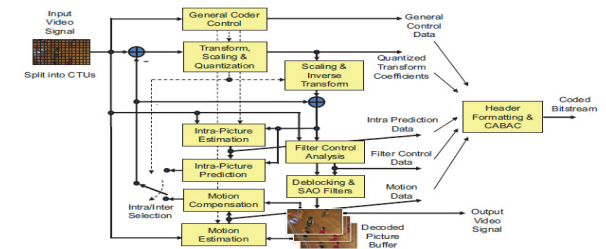
➤ Software Defined Radio (SDR): Wireless systems based on the embedded system platform (e.g. OMAP, WARP)



^α sponsored by National Science Council: NSC 101-2218-E-011-045

^α Collaboration with University of California, Irvine

Current Project II: Algorithms and Architectures for HEVC (High Efficient Video Coding)



➤ Next-generation Video compression:

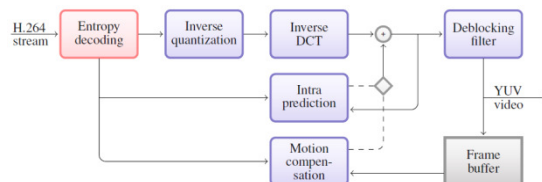
- Much improved coding efficiency with lower bit rate
- Requires advanced signal processing tools and techniques

➤ The design of efficient signal processing algorithms:

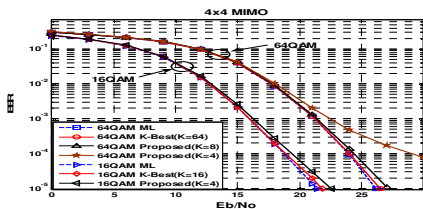
- Deblocking filter, Sample-adaptive offset filter, Quadtree-based partitioning and merging ...etc

➤ VLSI architectures and embedded multimedia systems:

- Digital circuits design
- DSP-based system / Multi-core architectures



Research/Design Flow



Algorithm Development

- Verify performance
- **C** or **Matlab** simulation

VLSI flow

Embedded System flow

- **RTL** design
- **Verilog** HDL

Architecture Design

Software Optimization

- **Embedded processors architecture**
- E.g. **DSP, ARM**

- **ASIC** design flow
- **FPGA** platform

Verification

Verification

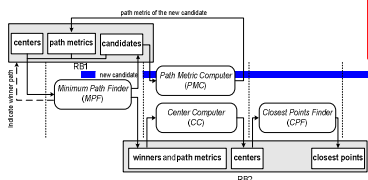
- **Embedded platform**
- E.g. **TI DaVinci, OMAP**

Job opportunities

- Researcher
- Algorithm developer
- Architecture developer
- Digital IC designer

- Researcher
- Algorithm developer
- Firmware engineer

Job opportunities



Prior Achievements

- A MIMO detection algorithm and the detector was designed and implemented on FPGA and to ASIC. [*IEEE CCNC 2010 ; IEEE TVLSI 2010 ; IEEE TCAS-I, 2010*]
 - The algorithm, architecture, and implementation of MIMO detectors that support hard and soft decision are realized. [*IEEE ISCAS 2010 ; IEEE TVLSI, 2012*]
 - An algorithm and VLSI architecture of joint MIMO detection and decoding of convolutional codes was designed and implemented. To the best of our knowledge, this is the first design to present the algorithm and VLSI architecture for such joint structure. [*IEEE TCAS-I, 2012*]
 - An error resilient MIMO detection algorithm for memory-dominated wireless communication systems was designed [*IEEE Globecom, 2012*]
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Publication List

Journals

- [J1] C. P. Sukumar, **C.-A. Shen**, and A. M. Eltawil, " Joint Detection and Decoding for MIMO Systems Using Convolutional Codes: Algorithm and VLSI Architecture," *IEEE Transactions on Circuits and Systems-I*, vol.59, no.9, pp. 1919-1931, Sep. 2012.
- [J2] **C.-A. Shen**, A. M. Eltawil, S. Mondal, and K. N. Salama, " A Best-First Soft/Hard Decision Tree Searching MIMO Decoder for a 4 x 4 64-QAM System," *IEEE Transactions on VLSI Systems*, vol. 20, no. 8, pp. 1537-1541, Aug. 2012.
- [J3] S. Mondal, A. M. Eltawil, **C.-A. Shen**, and K. N. Salama, "Design and Implementation of a Sort Free K-Best Sphere Decoder," *IEEE Transactions on VLSI Systems*, vol. 18, no. 10, pp. 1497-1501, Oct. 2010.
- [J4] **C.-A. Shen** and A. M. Eltawil, " A Radius Adaptive K-Best Decoder with Early Termination: Algorithm and VLSI Architecture," *IEEE Transactions on Circuits and Systems-I*, vol. 57, no. 9, pp. 2476-2486, Sep. 2010.
- [J5] **C.-A. Shen**, K. N. Salama, and A. M. Eltawil, " Evaluation Framework for K-Best Sphere Decoders," *Journal of Circuits, Systems, and Computers*, vol. 19, no. 5, pp. 975-995, Aug. 2010.

Conferences

- [C1] M. K. Khairy, **C.-A. Shen**, A. M. Eltawil, and F. Kurdahi, " Error Resilient MIMO Detector for Memory-Dominated Wireless Communication Systems," to appear in IEEE Global Communications Conference (Globecom), Dec. 2012.
- [C2] **C.-A. Shen**, A. M. Eltawil, S. Mondal, and K. N. Salama, " A Best-First Tree-Searching Approach for ML Decoding in MIMO System," in proceedings of *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 3533-3536, 2010.
- [C3] **C.-A. Shen** and A. M. Eltawil, "An Adaptive Reduced Complexity K-Best Decoding Algorithm with Early Termination," in *proceedings of IEEE Consumer Communications and Networking Conference(CCNC)*, pp. 1-5, 2010.
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Short Bio

Chung-An Shen is an Assistant Professor at National Taiwan University of Science and Technology. He received the PhD degree in ECE from University of California, Irvine in 2012, the M.Sc. In EE from The Ohio State University, Columbus in 2003, and the B.Sc. In EE from National Taiwan University of Science and Technology in 2000. Since 2012, he has been with the Department of Electronic and Computer Engineering, National Taiwan University of Science and Technology. His current research interests are in the field of algorithms and VLSI architectures design for signal processing systems with a focus on communication and video processing systems. Dr. Shen actively participates in professional service including reviewing articles for journals such as IEEE TCAS-I, II, TVLSI, and conferences including ICECS and VTC. Dr. Shen also held several industry positions before joining NTUST, including DSP instructor in Texas Instruments, Taipei, Taiwan, Intern Engineer in Mindspeed Technologies, Irvine, CA, USA, and Senior Firmware Design Engineer in Qualcomm Inc., San Diego, CA, USA.
