



Optoelectronics and Semiconductor Group

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I. The Subject and Aims of Research

1. Power semiconductor device design and process development— to study the process simplification scheme for power device , and also develop a dual-doped body regime to improve the conducting characteristics. In addition , IGBT with blocking voltage over 600 volts is designed.
2. sub-0.1 um IC process and device— to study the design of sub-0.1um MOSFET device formed on bulk and SOI Si substrate, also including the channel and drain engineering. In addition, the gate, source/drain junction, and high-k capacitors are also investigated.
3. Nano-device and process— to study the growth mechanism of Si nano-wires, and to form a tri-terminal transistor in self-aligned process.
4. Display device and technology— to achieve high-performance TFT by using large-angle-tilt-implanted drian (LATID), and also study the effects of lightly-doped-drain implantation condition on device characteristics. In addition, channel engineering is also investigated. The buried channel structure is also formed to improve the device performance.
5. Solar cell device and process— to study the structure and process with respect to Si, SiGe, SiC, material, for achieving better conversion efficiency..

II.Recent Research Topics

Fabrication of trench-gate power MOSFET's by using a dual doped body region has been proposed to further improve the device performance. For the usual scheme that employs a uniform doped body region, a device with a blocking voltage larger than 30V and a specific on- state resistance of about 1.0 ohm-cm can be obtained via the proper choice of trench depth, epitaxial thickness, and body doping concentration. On the other hand, a dual doped body region is produced by dual high-energy and low-energy implantation of boron dopant. By this scheme, a device with a blocking voltage larger than 30 V and a specific on-state resistance of about 0.8 ohm-cm can be further achieved. Hence, with reducing the cell pitch size to be below 2 μm , this device fabrication scheme should be promising and practical for achieving a specific on-resistance smaller than 0.1 $\text{m}\Omega\text{-cm}^2$ and a blocking voltage higher than 30 V.

A novel poly-Si TFT formed by using the large-angle-tilt-implanted-drain (LATID) scheme has been proposed. The LATID TFT can achieve much smaller off-state leakage than the lightly-doped-drain (LDD) TFT. The result is attributable to the reduced electric field near the drain region and thus more effective suppression of carrier emission via trap states. Moreover, the on-state current does not have large difference in comparison with the LDD TFT, due to the gate-overlapped structure formed by using simple fabricating process. As a result, a poly-Si TFT with excellent

device characteristics and high on/off current ratio can be implemented by simply using the LATID fabrication scheme.

III. Publication

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