Computer Engineering Group
Assistant Professor Mon-Chau Shie

Ph.D., National Taiwan University
Field of study: Embedded System, Operating System, FPGA Digital System Design, Video Coding
Key words: Embedded System, SoPC, Video Coding
URL: http://www.et.ntust.edu.tw/people/detail/b-06.htm
Email: mice@et.ntust.edu.tw
Phone: 886-2-27376398

1.The Subject and Aims of Research

- Embedded System: Embedded system platform development.
- Operating System: Research of O.S. operating mechanism.
- FPGA Digital Design: Digital system and hardware architecture.
- Video Coding: Research of video coding algorithm.

2.Related Recent Research Topics

(1) A Study of Fast Video Coding Algorithm

Video coding is a very computation-intensive computation. With the quality requirement of motion pictures gets higher and higher, but storage media is capacity limited, we need more efficient algorithm to codes video without losing its quality. This research focuses on the algorithms of video coding, and to analyze efficiencies of various algorithms. We develop new algorithms to improve compression efficiency without losing its quality, even better quality and less compressed data. We also develop its VLSI architecture for its feasibility and usability.

(2) A Study of FPGA Based VLSI Architecture

In this topic, we discuss the fast prototyping of VLSI, to see the possibility of any architecture. We study the best optimized VLSI architectures for dedicate algorithms. We also discuss the possibility of implementation or what architectures is the most suitable for any specific FPGA. The study of existing prototypes also inspires us new ideas for other prototypes.

(3) Development of Embedded System

Microprocessor is the main stream of modern microcomputer. With the mass improvement of performance of modern CPU and peripherals, popularity of Internet access, and high performance computing requirements, traditional 8051 based microprocessor system is no longer suitable. We develop 32-bit RISC based embedded system with small memory and integrated I/O. In addition to hardware development, we also develop software of embedded system, including Boot Loader, Board Support Package, and device driver for custom hardware, to construct a complete embedded system from inside out.

3.Selected Publications and Projects

Publications:

[1]**Mon-Chau Shie**, Wen-Hsien Fang, Kuo-Jui Hung, Feipei Lai, "Fast, Robust Block Motion Estimation Using Simulated Annealing," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol.E83-A, no.1, pp.121-127. January. 2000 (SCI/EI)

[2]Chi-Chia. Sun, Shanq-Jang Ruan, **Mon-Chau Shie** and Tun-Wen. Pai, "Dynamic Contrast Enhancement based on Histogram Specification," IEEE Trans. Consumer Electronics. (to appear in Nov. 2005) (SCI/EI)

[3] Chi-Chia Sung, Shanq-Jang Ruan, Bo-Yao Lin, and **Mon-Chau Shie**, "Quality and Power Effcient Architecture for the DiscreteCosine Transform" IEICE Trans. on Fundamentals," vol. E88-A, no. 12, Dec. 2005 (SCI/EI)

[4] Po-Hung Chen, Hung-Ming Chen, Kuo-Jui Hung, **Mon-Chau Shie,** and Feipei Lai, "A robust fuzzy reasoning based algorithm for fast block motion estimation," *The 2002 IEEE International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS'02)**:** Fuzzy Systems*, Nov. 21-24, 2002, Kaoshiung, Taiwan,.

[5] Po-Hung Chen, Kuo-Liang Yeh, **Mon-Chau Shie** and Feipei Lai, "BITCEM: An adaptive block motion estimation based on center of mass object tracking via binary transform," *The 2001 IEEE International Symposium on Signal Circuits and System (SCS'01): Image Processing, Jul. 10-11, 2001, Iasi, Romania.*

[6] Po-Hung Chen, Kuo-Liang Yeh, **Mon-Chau Shie** and Feipei Lai, "Fast block matching algorithm based on video motion type using BITCEM object tracking technique," *The 2001 IEEE International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS'01): Digital Video Processing,* Nov. 20-21, 2001, Nashville, Tennessee, USA.

[7] Po-Hung Chen, Kuo-Jui Hung, **Mon-Chau Shie**, Wen-Hsien Fang, and Feipei Lai, "Markov model Fuzzy-Reasoning based algorithm for Fast Block Motion Estimation," (2005 JVCIR to be appeared)

[8] Bo-Yao Lin, Chi-Chia Sung, Shanq-Jang Ruan, and **Mon-Chau Shie** "A Novel DCT architecture for Quality and Power Efficient" IEEE International Workshop on Nonlinear Signal and Image Processing (NSIP 2005), May 2005.