All-Digital Time-Domain Smart Temperature Sensor With an Inter-Batch Inaccuracy of $-0.7\ ^\circ\mathrm{C} - +0.6\ ^\circ\mathrm{C}$ After One-Point Calibration

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***Abstract*—To get rid of the heavy burden of aspect ratio tuning, bias adjustment and porting problem among processes in full-custom or mixed-mode design, a fully digital smart temperature sensor realizable with 140 field programmable gate array (FPGA) logic elements was proposed for painless VLSI on-chip integrations. By simply replacing the cyclic delay line with a retriggerable ring oscillator for accuracy enhancement, modifying the gain of time amplifier from fixed to variable for one-point calibration support and adopting a second-order master curve for curvature correction in this paper, the proposed smart temperature sensor can achieve two thirds reduction in circuit size, at least four-fold improvement in power consumption and more than two-fold enhancement in accuracy. To demonstrate the performance under practical process variation, the sensor realized with as few as 48 FPGA logic elements for rapid prototyping was measured over 0 °C to 100 °C range for 20 test chips from batches spreading over 4 years. The measured inaccuracy is $-0.7\ ^\circ\mathrm{C} - +0.6\ ^\circ\mathrm{C}$ which is superior to $-1.8\ ^\circ\mathrm{C} - +2.3\ ^\circ\mathrm{C}$ of its full-custom predecessor with a third-order master curve and five test samples from one single batch. The accuracy is even better than those of full-custom sensors with two-point calibration. The conversion rate is around 4.4 kHz and the power consumption can be reduced to 175 nJ per conversion by increasing the number of delay stages in ring oscillator to 4608.**

***Index Terms*—Field programmable gate array (FPGA), fully digital, smart temperature sensor, time-domain, variable-gain time amplifier (VGTA).**

I. Introduction

NOWADAYS, there is an incredible growth in sensor network, bio/on-chip thermal sensing, temperature monitoring, temperature drift compensation, processor speed control, and power management markets [3]–[8]. The demand for low-cost but high-accuracy smart temperature sensors becomes stronger than ever. To enhance battery durability, low power consumption is also required in battery-powered systems. The power restriction is even demanding for RF-powered applications [9]. In addition, small chip size and CMOS fabrication are necessary for most embedded applications.

Conventionally, test temperature was converted by a thermal sensor into a voltage signal first, and then a corresponding ADC was utilized for subsequent output coding [3]. The usual expense was large chip size and tremendous power consumption. After years of evolving, a state-of-the-art smart temperature sensor was presented to successfully reduce measurement inaccuracy from $\pm 1\ ^\circ\mathrm{C}$ over $-40\ ^\circ\mathrm{C} - +120\ ^\circ\mathrm{C}$ temperature range after two-point calibration [3] to $\pm 0.1\ ^\circ\mathrm{C}\ (3\sigma)$ over $-55\ ^\circ\mathrm{C} - 125\ ^\circ\mathrm{C}$ temperature range [10]. The price was individual transistor trimming after packaging, 4.5-mm^2 die area and 75-μA current consumption in a 0.7-μm CMOS process. Significant cost savings could be obtained by batch calibration, but it was usually accompanied by an equally significant loss of accuracy [11]. The error became $\pm 0.25\ ^\circ\mathrm{C}\ (3\sigma)$ from $-70\ ^\circ\mathrm{C}$ to 130 °C and the consumption current was 25 μA in the same CMOS process. With similar accuracy, a seven-fold energy saving could be accomplished by utilizing a zoom ADC that combined a coarse SAR conversion with a fine $\Delta\Sigma$ conversion [12]. Without any calibration or trimming, a 32-nm CMOS temperature sensor achieved an inaccuracy less than 5 °C from $-10\ ^\circ\mathrm{C}$ to 110 °C successfully [13]. However, the power consumption was as high as 1.6 mW.

With large chip size or high power consumption, most conventional voltage-domain smart temperature sensors were less attractive to low cost or low power VLSI on-chip temperature sensing. One feasible way for cost down is to compose time-domain smart temperature sensor [14]. The sensor converted the test temperature into a time signal with a thermally sensitive width first and then utilized a time-to-digital convertor (TDC) which could be much simpler and more power efficient than ADC for output coding. A delay line which consumed less power and chip size was usually adopted to be the temperature-to-time generator. However, the expense was comparatively poor accuracy. The power consumption and chip size were substantially reduced to 10 μW@2 Sa/s and 0.175 mm^2 in a 0.35-μm digital CMOS process with a measurement error of $-0.7\ ^\circ\mathrm{C} - +0.9\ ^\circ\mathrm{C}$ from 0 °C to 100 °C after two-end-point calibration. By comparing the frequencies of two current-starved ring oscillators based on a temperature insensitive current source and a proportional to absolute temperature (PTAT) current source, respectively, the power consumption and chip

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