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Field of study: Integrated Circuit Design
Key words: Data Conversion, Biomedical Analog Front-End Circuit, Phase-Locked Loop
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1. The Subject and Aims of Research

Research interests include high-speed data converters, ultra-low power data converters, digital calibration techniques, phase-locked loop, biomedical analog front-end circuits and biomedical system designs.

2. Related Recent Research Topics

- High-Speed Data Converters

High-speed (>1GS/s) analog-to-digital converters (ADCs) are widely applied on measurement instruments, hard disk drive, blue-ray disk drive and next generation wireless communication systems (e.g. LTE). For less than 6-bit ADCs, flash architecture is generally applied. But for an 8-bit ADC, subranging architecture cannot operate to achieve 1GHz sampling rate due to its intrinsic architecture limitation. Folding ADCs use pre-amplifiers to process input signal but consume large power. In order to breakthrough such limitation, we may use the advantage of nanometer transistors, high-speed and low power, to design a new 8-bit, larger than 1GHz sampling rate ADC to meet both high-speed and low power consumption.

- Ultra-Low Power Data Converters

By CMOS scaling, transistor's operation speed becomes faster. This makes successive-approximation register (SAR) architecture more suitable to implement 10-bit and below 100MS/s ADCs. It uses the strength of nanometer transistors, high-speed and low power, to achieve ultra-low power consumption. However, for higher resolution (≥12-bit) ADCs, the capacitor mismatch brings new challenge to mitigate the strength of SAR architectures. For example, we usually uses capacitor array to implement the DAC in a SAR ADC. Higher resolution requires large capacitance to reduce the DAC error due to the capacitor mismatch. This will increase power consumption. Here our target is to propose new techniques to reduce the capacitance in the DAC and total power consumption.

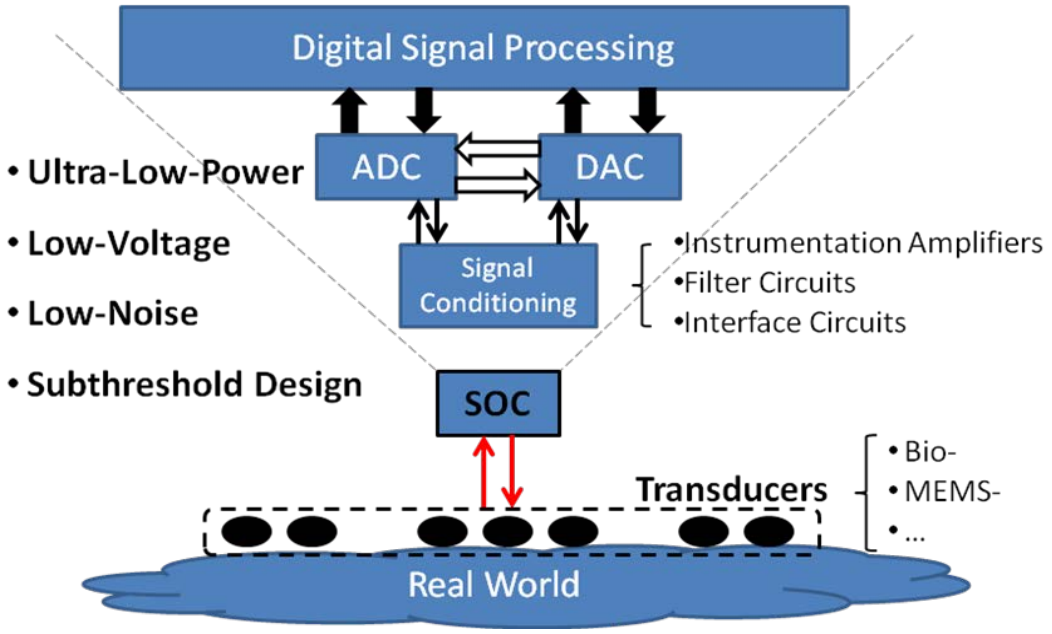
- Digital Calibration Techniques

This project is to develop new digitally-enhanced ADC techniques. These techniques can improve the ADC resolution without using highly linear analog circuits, which are difficult to implement with nanometer transistors. As you can see, transistors' supply voltage and intrinsic gain are lower by CMOS scaling (e.g. VDD=1V). Both of them are not good to implement high precision analog circuits. On the other hand, transistor's speed is faster. If the digital circuits can help the

analog circuits, a high-speed and high-resolution ADC can be implemented by breaking the analog limitation. It will be helpful to implement low-power electronic products in human life.

- Biomedical Analog Front-End Circuits

For biological measurements, ECG, EEG and EMG, wireless sensor network (WSN) or high-end medical instruments, instrumentation amplifiers and data converters play important roles to determine the system specification and capability of competition. Biomedical analog front-end circuits are highly dependent on their system platforms. It's necessary to customize a sensor interface circuit for biomedical application and use core technologies to determine the circuit architecture. That will introduce an optimized biomedical sensor interface to capture high quality biomedical signals.



3. Publications

Journal papers

[1] Yung-Hui Chung and Jieh-Tsorng Wu, “A CMOS 6-mW 10-bit 100-MS/s Two-Step ADC,” *IEEE J. Solid-State Circuits*, vol. 45, no. 11, pp. 2217–2226, Nov., 2010.

Conference papers

[1] Yung-Hui Chung*, Meng-Hsuan Wu, and Hung-Sung Li, “A 24μW 12b 1MS/s 68.3dB SNDR SAR ADC with Two-Step Decision DAC Switching,” in Proc. *IEEE Custom Integrated Circuits Conference* (CICC), Sep. 2013, pp. 1–4.

[2] Yung-Hui Chung*, “The Swapping Binary-Window DAC Switching Technique for SAR ADCs,” in Proc. of IEEE Int. Sym. on Circuits and Systems, ISCAS, May, 2013, pp.2231-2234.

[3] Meng-Hsuan Wu, Yung-Hui Chung*, and Hung-Sung Li, “A 12-bit 8.47-fJ/Conversion-Step 1-MS/s SAR ADC using Capacitor-Swapping Technique,” in Proc. *IEEE Asian Solid-State Circuits Conf.*, Nov., 2012, pp.157-160.

[4] Yung-Hui Chung* and Jieh-Tsorng Wu, “A 16mW 8-bit 1-GS/s Subranging ADC in 55nm CMOS,” in *VLSI Circuits Symp. Dig.*, Jun. 2011, pp.128–129.

[5] Yung-Hui Chung* and Jieh-Tsorng Wu, “A CMOS 6-mW 10-bit 100-MS/s Two-Step ADC,” in Proc. *IEEE Asian Solid-State Circuits Conf.*, Nov. 2009, pp.137-140.